

Space product assurance

ASIC/FPGA development

FINAL DRAFT STANDARD

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Foreword

This Standard is one of the series of ECSS Standards intended to be applied together for the management, engineering and product assurance in space projects and applications. ECSS is a cooperative effort of the European Space Agency, national space agencies and European industry associations for the purpose of developing and maintaining common standards.

Requirements in this Standard are defined in terms of what shall be accomplished, rather than in terms of how to organize and perform the necessary work. This allows existing organizational structures and methods to be applied where they are effective, and for the structures and methods to evolve as necessary without rewriting the standards.

The formulation of this Standard takes into account the existing ISO 9000 family of documents.

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CONTENTS	PAGE
Foreword.....	3
Introduction.....	7
1. Scope	9
2. Normative references.....	11
3. Terms, definitions and abbreviated terms.....	13
3.1 Terms and definitions.....	13
3.2 Abbreviated terms.....	15
4. ASIC/FPGA programme management.....	17
4.1 General	17
4.1.1 Organisation	17
4.1.2 Planning.....	17
4.2 ASIC/FPGA control plan	17
4.3 Management planning tools.....	18
4.3.1 ASIC/FPGA development plan.....	18
4.3.2 Verification plan	18
4.3.3 Design validation plan	18
4.4 Experience summary report.....	18
5. ASIC/FPGA engineering	19
5.1 General	19
5.2 Definition phase	22
5.2.1 General.....	22
5.2.2 Identification of ASIC/FPGA requirements.....	22
5.2.3 Feasibility and risk assessment.....	23
5.2.3.1 Feasibility study.....	23
5.2.3.2 Risk analysis	23
5.2.4 ASIC/FPGA development plan.....	24
5.2.5 Initial design review	25
5.2.6 Outputs	26
5.3 Architectural design.....	27
5.3.1 General.....	27
5.3.2 Architecture definition.....	27
5.3.3 Verification plan	28
5.3.4 Architecture verification and optimisation.....	28
5.3.5 Preliminary data sheet.....	28
5.3.6 Architectural design review	28
5.3.7 Outputs	29
5.4 Detailed design	29
5.4.1 General.....	29
5.4.2 Design entry	29
5.4.3 Netlist generation	30
5.4.4 Netlist verification	30
5.4.5 Updated data sheet	31
5.4.6 Preliminary design review	31
5.4.7 Outputs	32
5.5 Layout	32
5.5.1 General.....	32
5.5.2 Layout generation.....	33

ECSS-Q-60-02

5.5.3	Layout verification	33
5.5.4	Design validation plan	34
5.5.5	Updated data sheet	34
5.5.6	Draft detail specification	34
5.5.7	Critical design review	34
5.5.8	Outputs	35
5.6	Prototype implementation	35
5.6.1	General.....	35
5.6.2	Manufacture/programming and test	35
5.6.3	Outputs	35
5.7	Design validation and release.....	37
5.7.1	Design validation	37
5.7.2	Radiation test performance	37
5.7.3	Design release and FM production preparation	37
5.7.4	Experience summary report	38
5.7.5	Final versions of application and procurement documents	38
5.7.6	Design validation review.....	38
5.7.7	Outputs	38
6.	Quality assurance system	40
6.1	General	40
6.2	Review meetings.....	40
6.3	Risk assessment and risk management	42
6.4	Supplier dependability.....	42
7.	Development documentation	44
7.1	General	44
7.2	Management documentation	44
7.2.1	General.....	44
7.2.2	ASIC/FPGA control plan.....	44
7.2.3	ASIC/FPGA development plan.....	44
7.2.4	Minutes of review meetings.....	45
7.2.5	Verification plan	45
7.2.6	Design validation plan	45
7.2.7	Experience summary report	45
7.3	Design documentation	45
7.3.1	General.....	45
7.3.2	Definition phase documentation	47
7.3.3	Architectural design documentation	47
7.3.4	Detailed design documentation	47
7.3.5	Layout documentation	48
7.3.6	Design validation documentation	48
7.4	Application and procurement documents.....	49
7.4.1	Data sheet	49
7.4.2	Application note	49
7.4.3	Detail specification	50
8.	Deliverables.....	52
8.1	General	52
8.2	Deliverable items.....	52
8.3	Acceptance of deliverable items	54
Annex A	55

Informative references 55

Introduction

The added responsibilities of developing custom designed devices, as opposed to using off-the-shelf components, make certain management activities crucial to the success of the procurement programme. This was already considered by the applicable Standard for “Space Product Assurance of EEE Components” ECSS-Q-60 that classifies custom designed devices such as ASIC components under “Specific Components” for which specific requirements are applicable.

For space projects the requirements for development of custom designed components described in this Standard present guidelines for the customer to define his requirements in line with this standard and to accept appropriate clauses for the Project Requirements Document (PRD).

The supplier defines requirements for development of custom designed components within the boundaries of this standard based on the requirements of the system and its elements, and takes into consideration the operational and environmental requirements of the programme.

The supplier also defines an ASIC/FPGA Control Plan to implement those requirements into a system which enables to control the technology selection, design, synthesis and simulation, layout, design validation, etc. in a schedule compatible with his requirements, and in a cost-efficient way.

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1. Scope

This Standard defines a comprehensive set of requirements for the successful development of digital, analog and mixed analog-digital custom designed integrated circuits such as Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). The development includes all activities starting by setting initial requirements and ending with the validation and release of prototype devices.

This Standard is aimed at ensuring that the custom designed components used in space projects meet their requirements in terms of functionality, quality, reliability, schedule and cost. The support of appropriate planning and risk management is needed to ensure that each stage of the development activity is consolidated before starting the subsequent one and to minimise or avoid additional iterations. For the development of standard devices such as Application Specific Standard Products (ASSPs) or IP Cores additional requirements might have to be considered which are not in the scope of this document.

The principal sections of this Standard correspond to the main concurrent activities of a circuit development programme that are:

- ASIC/FPGA programme management
- ASIC/FPGA engineering
- ASIC/FPGA quality assurance

The provisions of this document apply to all actors involved in all levels in the realisation of space segment hardware and its interfaces.

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2. Normative references

The following documents, of the latest issue, form part of this document to the extent specified herein:

ECSS-P-001	ECSS glossary of terms
ECSS-M-40	Space product Management, Configuration Management
ECSS-Q-00	Space product assurance, Policy and principles
ECSS-Q-20	Space product assurance, Quality assurance
ECSS-Q-30	Space product assurance, Dependability
ECSS-Q-60	Space product assurance, EEE Components

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3. Terms, definitions and abbreviated terms

3.1 Terms and definitions

The following terms and definitions are specific to this Standard in the sense that they are complementary or additional with respect to those contained in ECSS-P-001 and ECSS-Q-60.

3.1.1

Application Specific Integrated Circuit (ASIC)

a full custom or semi custom designed monolithic integrated circuit that may be digital, analog or a mixed function for one user

3.1.2

ASIC Technology

totality of all elements required for the design, manufacture and test of ASIC components such as design tools and their description, cell libraries, procedures, design rules, process line and test equipment.

3.1.3

Application Specific Standard Products (ASSP)

ASSPs are ASICs designed to make standard products that are generally made available to a broader range of applications and most often are provided with a VHDL model and disseminated with documentation.

3.1.4

Block Diagram

abstract, graphical presentation of interconnected, named boxes (blocks) representing an architectural/functional drawing

3.1.5

Cell

specific circuit function including digital and/or analog basic blocks.

3.1.6

Cell Library

collection of all mutually compatible cells which conforms to a set of common constraints and standardised interfaces designed and characterised for a specified technology.

3.1.7

Data Sheet

detailed, functional, operational and parametric description of a component including block diagram, truth table, pin/signal description, environmental, electrical and performance parameters, tolerances, timing information, package description, and others

3.1.8

Design Flow

selection and sequence of engineering methods and tools to be applied during the implementation of the design.

3.1.9

Design for Test (DFT) Structure

technique used to allow a complex IC to be tested which may include any mechanism aimed to provide better observability and/or commandability of internal nodes of the chip not accessible through primary inputs and outputs.

3.1.10

Design Iteration

design changes which occur in any single phase or between two consecutive phases as defined in the ASIC/FPGA Development Plan, before the design has been released for prototype implementation.

3.1.11

Detail Specification

procurement specification according to ESA/SCC format that defines the maximum ratings, parameter limitations, mechanical outline, pin description, screening requirements, etc..

3.1.12

Development Step

major step of the development flow for the ASIC/FPGA development such as Definition Phase, Architectural Design, Detailed Design, Layout, Prototype Implementation and Design Validation.

3.1.13

Fault Coverage

measure, expressed in percentage terms, of the proportion of actually detectable versus all possible faults in a digital circuit, for a given set of test patterns and with respect to a specific fault model.

3.1.14

Field Programmable Gate Array (FPGA)

standard semiconductor device that becomes customised when programmed by the user with the FPGA vendor specific software and hardware tools.

3.1.15

Floorplan

abstracted, scaled layout drawing of the die, outlining the form, size and position of the major functional blocks and the pads including power/ground lines, clock distribution and interconnect channels.

3.1.16

HDL

term used in general for the various "Hardware Description Languages" which are applied for coding during design phase such as VHDL, Verilog, and others.

3.1.17

HDL Model

textual model based on a hardware description language suitable for the behavioural and/or structural description, simulation and by choosing a suitable level of abstraction for automatic netlist generation.

3.1.18

Intellectual Property (IP) Core

design element that implements a self-standing function or group of functions for which ownership rights exist and that can be acquired by a customer, for a given price and under an owner-defined license agreement specifying the customer's acquired rights, to be used, for example, as a building block for another design. It is normally expected to be supplied as an HDL file (e.g. synthesisable VHDL code or gate-level netlist) and with the essential complementary documentation that would allow the customer to successfully integrate and use it in a system (User's Manual, verification files, etc.).

3.1.19

Macrocell

module that contains complex functions in a vendor's cell library built up out of hard-wired primitive cells.

3.1.20

Netlist

formatted list of cells (basic circuits) and their interconnections.

3.1.21

Prototype Device

fabricated ASIC or programmed FPGA used to validate the new design in respect to functionality, performance, operation limits and compatibility with its system.

3.1.22

Redesign

design changes which affect more than two consecutive phases of the ASIC/FPGA development or design changes that are implemented after prototype implementation.

3.1.23

Stimuli

input data set for simulation or test to show a specific functionality or performance of a device.

3.1.24

Test Pattern

simulation stimuli and its expected responses (considering specific constraints to meet test equipment requirements) used to show correct behavior of a device.

3.2 Abbreviated terms

The following abbreviated terms are defined and used within this Standard.

Abbreviation	Meaning
ACP	ASIC/FPGA Control Plan
ADP	ASIC/FPGA Development Plan
ADR	Architectural Design Review
ARS	ASIC/FPGA Requirements Specification
ASCII	American Standard Code
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
CAD	Computer-aided Design
CDR	Critical Design Review
DD	Design Documentation
DFT	Design for Test
DRC	Design Rule Check
DVP	Design Validation Plan
DVR	Design Validation Review

ECSS-Q-60-02

EDA	Electronic Design Automation
EDAC	Error Detection and Correction.
EDIF	Electronic Design Interchange Format
EM	Engineering Model of a Prototype
ERC	Electrical Rule Check
ESA/SCC	European Space Agency/Space Components Coordination
FM	Flight module part
FPGA	Field-programmable Gate Array
FRR	Feasibility and Risk analysis Report
GDS	Graphic Design System (industry standard graphics entry tool)
HDL	Hardware Description Language
IDMP	Input Data for Mask or Programming file generation
IDR	Initial Design Review
IEEE	Institute of Electrical and Electronics Engineers
IP	Intellectual Property
IPO	In-Place Optimisation
MoM	Minutes of Meeting
P&R	Place and Route
JTAG	Joint Test Action Group
LVS	Layout vs. Schematic Check
NCC	Netlist Comparison Check
PDR	Preliminary Design Review
QM	Qualified Model of a Prototype
QML	Qualified Manufacturer List
RTL	Register Transfer Logic
SEU	Single Event Upset
SMD	Standard Microcircuit Drawing
SOW	Statement of Work
SRAM	Static Random Access Memory
TMR	Triple Modular Redundancy
US QML	US Qualified Manufacturer List
VHDL	VHSIC Hardware Description Language, as defined in IEEE 1076.
VHSIC	Very High Speed Integrated Circuit (US Government research programme)
VLSI/ULSI	Very/Ultra Large Scale Integration

4. ASIC/FPGA programme management

4.1 General

The supplier shall establish and implement throughout the duration of the contract an ASIC/FPGA Programme as part of the Component Programme (see ECSS-Q-60) which ensures full compliance with the requirements of the project as defined by his customer in line with this standard.

4.1.1 Organisation

The supplier shall establish and maintain an organisation responsible for the management of the ASIC/FPGA Programme. This organisation shall comply in all respects with the requirements of ECSS-Q-00 subclauses 3.3.1 (Responsibility and Authority) and 3.3.2 (Resources). In case of major problems the development team as allocated in the development plan (see para. 4.3.1) shall be obliged to directly report to the Component Advisory Board.

4.1.2 Planning

The supplier shall ensure that the ASIC/FPGA developments that are necessary for the implementation of the ASIC/FPGA Programme are thoroughly planned, documented and implemented in timely manner and that preventive / corrective actions are initiated whenever there is evidence of possible schedule or technical problems.

4.2 ASIC/FPGA control plan

The supplier shall prepare an ASIC/FPGA Control Plan (ACP) which initiates the ASIC/FPGA developments and specifies the organisation, management tools, quality assurance system, strategy, approaches and procedures he will adopt. Specifically, this plan shall include, but not be limited to, a description of the following items:

- a. Organisational structure and management approach including the definition of organisational interfaces to optimise the work between different design groups and identification of a person responsible for the product assurance of the ASIC/FPGA development;
- b. Management tools to be applied for planning (see chapter 4.3) and quality assurance system (see chapter 6) of the ASIC/FPGA developments;
- c. Intended overall schedule;
- d. Overall strategy and general approach for the ASIC/FPGA developments;
- e. Risk mitigation procedures to be applied (see chapter 6.3)
- f. Requirements on, and system for the control of the foundry and other subcontractors or service providers involved according to the experience available for the respective contractor (see chapter 6.4);
- g. Compliance matrix to the clauses of this standard taking into account applicable tailoring as defined in the contract.
- h. Initiation of the Definition Phase for the ASIC/FPGA developments.

4.3 Management planning tools

4.3.1 ASIC/FPGA development plan

A detailed ASIC/FPGA Development Plan (ADP) shall be prepared, documented and maintained after the requirements are settled and the feasibility and risk for the ASIC/FPGA development is assessed. A detailed description of the ADP is given in chapter 5.2.4.

4.3.2 Verification plan

A Verification Plan shall be established, defining how the functionality and non-functional requirements stated in the Definition Phase Documentation shall be demonstrated at all levels of modelling. A detailed description of the Verification Plan is given in chapter 5.3.3.

4.3.3 Design validation plan

A Design Validation Plan (DVP) shall be established to specify the measurements that shall be performed on the prototypes in order to verify that the new implemented devices contain the functionality and the characteristic they are designed for. A detailed description of the DVP is given in chapter 5.5.4.

4.4 Experience summary report

In the frame of the supplier's continued quality improvement activities and to establish economic and efficient development and test requirements for expected future projects, the supplier should collect and evaluate continuously, and present in an experience summary report any relevant information resulting from the experience gained during the execution of the ASIC/FPGA development.

The Experience Summary Report, if required by the customer, shall include:

- a. A summary of the main design objectives and constraints;
- b. An assessment of the actual development programme (e.g. controls, schedule, design iterations, communications) with respect to the original ADP;
- c. An assessment of EDA tool suitability and performance;
- d. An assessment of the manufacturer support;
- e. A presentation of non-conformances and problem areas;
- f. In the case of usage of existing IP cores:
Experiences gained in terms of product quality and suitability: e.g., synthesis results, modelling, test stimuli, documentation, application support, problems encountered, etc.;
- g. Recommendations and lessons learned.

5. ASIC/FPGA engineering

5.1 General

This section covers the responsibilities of ASIC/FPGA managers and designers for the tasks essential to producing high-reliability circuit design and tests meeting all circuit function, test and performance requirements.

To consider the timely allocation of management and quality assurance activities to the engineering tasks, these activities are also specified within this section and clearly indicated as being a management or quality assurance activity.

All requirements and suggested tasks to be performed and documented throughout the entire ASIC/FPGA engineering activity are equally applicable, by default and unless indicated otherwise, to either case of integrated circuit option: DIGITAL, ANALOG or MIXED ASIC, as well as FPGAs. A few requirements do not apply to certain technology options, and this is indicated by attaching one or more of the following labels:

[D] Not applicable for digital ASIC designs;

[A] Not applicable for analog ASIC designs;

[F] Not applicable for FPGA designs;

The following general requirements shall be fulfilled:

- a. All inputs to the design, that are not automatically generated and are necessary to reproduce the design such as simulation pattern, schematics, VHDL source codes, synthesis scripts have to be put under a revision control mechanism agreed between the contractors;
- b. Each development step using design inputs has to report the revision numbers of the inputs in a log file to prove consistency;
- c. Each development step shall be verified by a mechanism as independent as feasible to guarantee its correct verification. The development step is completed when the step itself as well as its verification was performed and any error or serious warning being flagged by the tools was approved in the review meeting.

The ASIC/FPGA development flow is represented in Chart I below.

Chart I

Management/QA Documentation

Phases and Tasks

Design Documentation and Outputs

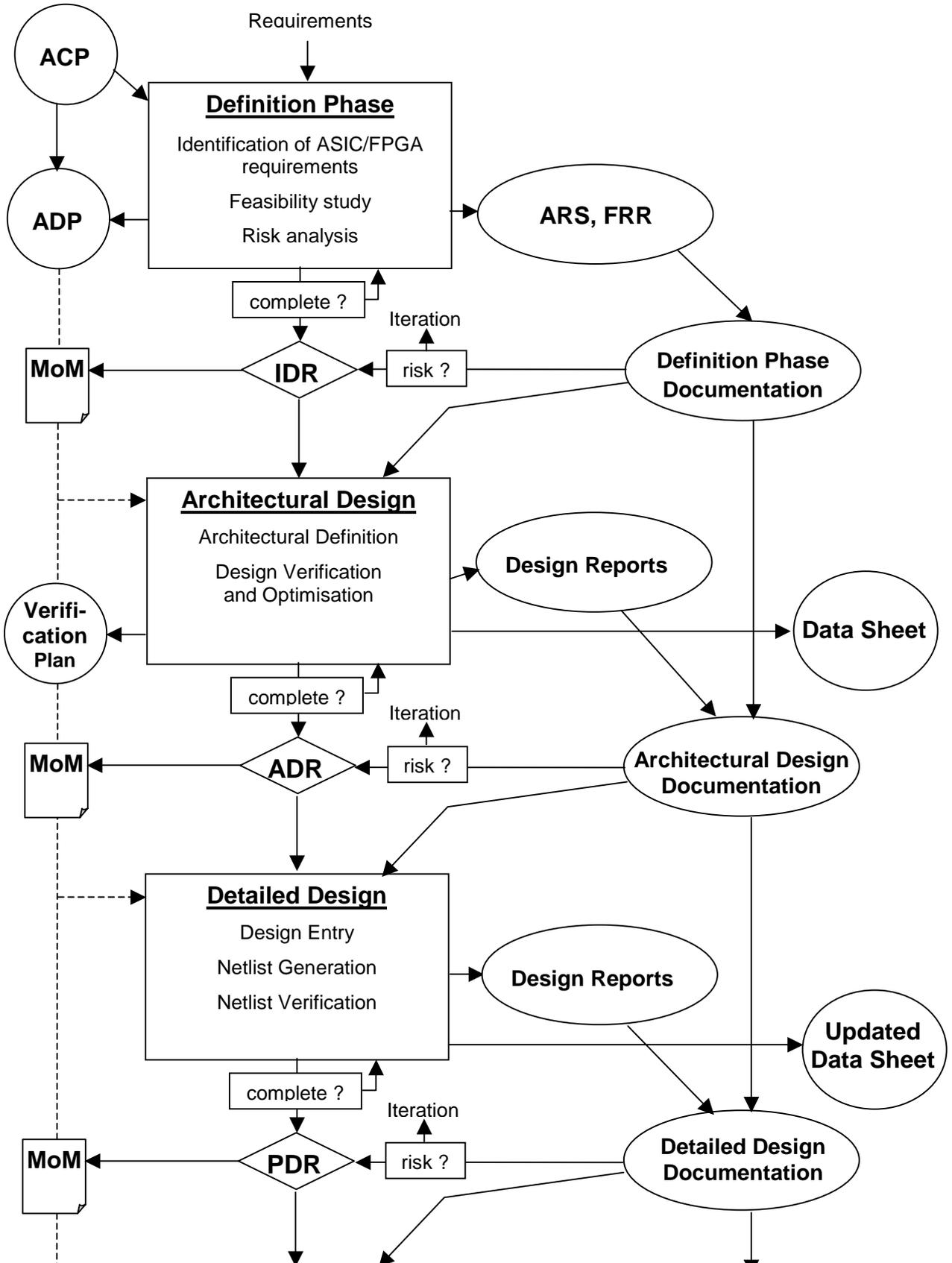
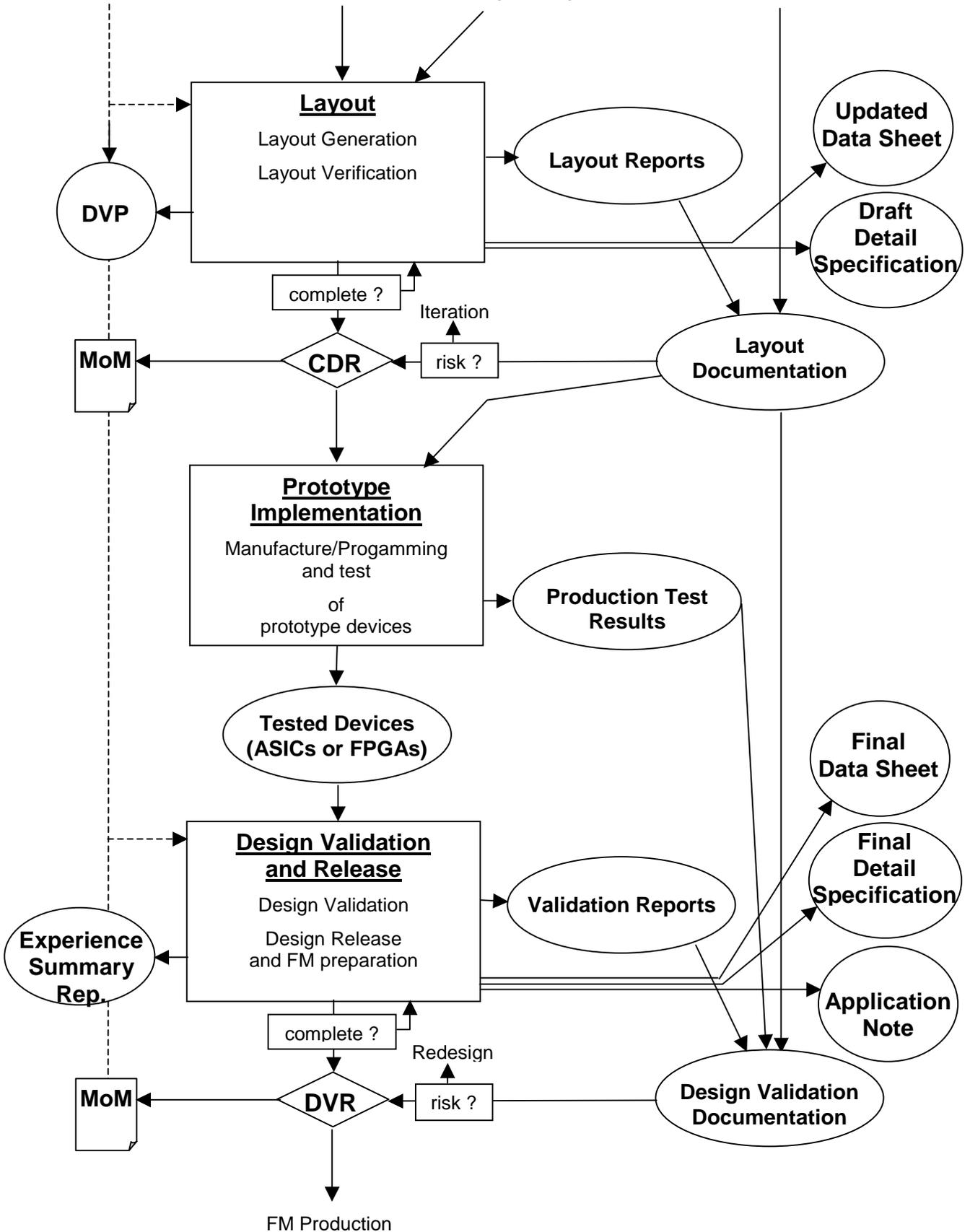


Chart I (Cont'd)



5.2 Definition phase

5.2.1 General

This phase shall ensure that all relevant system configurations and characteristics and all issues imposing requirements on the device are considered, that the definition status of the collected requirements is settled without any ambiguity and that all necessary resources for the design activities are available. The target of this development step is to establish an ASIC/FPGA Requirements Specification, a Feasibility and Risk Analysis Report and an ASIC/FPGA Development Plan.

5.2.2 Identification of ASIC/FPGA requirements

This task shall identify a complete set of ASIC/FPGA requirements which shall be documented in form of an ASIC/FPGA Requirements Specification (ARS), covering, as a minimum, the following items:

- a. Overall system partitioning, system configurations and operating modes;
- b. Interfaces of the ASIC/FPGA to the system and communication protocols to external devices, including memory mapping;
- c. Operating frequency range;
- d. Electrical constraints (e.g. voltage and current supply, drive capabilities, external load);
- e. Functional requirements;
- f. Applicable algorithms;
- g. Power-up and initialisation state;
- h. Reset and power cycling requirements;
- i. Error handling;
- j. Test modes: system and device tests, on ground and in flight;
- k. Fault coverage required at production test; **[A, F]**
- l. Timing of critical signals;
- m. Radiation environment constraints;
- n. Thermal environment constraints;
- o. Power budget and dissipation;
- p. Physical and mechanical constraints: pin assignment, size, encapsulation;
- q. Reusability and/or additional functions for future applications;
- r. Portability to different or newer technologies;
- s. Intellectual property rights of the design to be developed;
- t. Proprietary designs (IP cores) to be used as building blocks of the design to be developed, if already identified;

5.2.3 Feasibility and risk assessment

5.2.3.1 Feasibility study

The feasibility of the intended ASIC/FPGA development shall be assessed against the established ASIC/FPGA Requirements Specification and the available resources. As a minimum, the following tasks shall be performed and documented:

- a. Estimate design complexity;
- b. Estimate power consumption;
- c. Assess feasibility of speed requirements by a preliminary timing analysis;
- d. Select a radiation hardening approach that ensures compliance with radiation tolerance requirements. Determine a rough estimate of impact on chip area and/or circuit speed;
- e. Select a production test approach and its feasibility against all requirements;
- f. Identify and evaluate the suitability and qualification status of the ASIC technologies or FPGA available to implement the device, fulfilling all functional and non-functional requirements including the required derating factors. Make a baseline selection;
- g. Identify suitable packages, fulfilling all requirements. Make a baseline selection;
- h. Ensure that the baseline technology and package or FPGA have a remaining lifetime, so that flight and compatible prototype parts can be manufactured and/or are available during the expected procurement phase(s);
- i. Ensure that technical support for the device can be guaranteed during the expected lifetime;
- j. Determine availability and status of the required design and test tools (HW & SW) and libraries;
- k. Determine availability of the necessary human resources;
- l. Determine availability, licensing, support, legal and economical aspects of using IP cores from third parties;
- m. Ensure that no patents are infringed or agreements exist or can be made with the patent holder;

5.2.3.2 Risk analysis

As a tool of the quality assurance system (see chapter 6.3) a risk analysis shall be performed that identifies potential risk items and assigns preventive measures and contingency plans. As a minimum the following items shall be covered:

- a. Assurance that the collected ASIC/FPGA requirements are complete, settled and unambiguous;
- b. Maturity of foreseen ASIC or FPGA manufacturers and possible technologies;
- c. Experience and familiarity of engineering resources with the design type, tools, technology and the potential foundries;
- d. Risk of underestimation of design and verification effort;
- e. Risk of underestimation of debug and repair efforts;
- f. Risk of overestimation of actual gate capacity and clocking frequency;

- g. Risk of undetermined I/O behaviour during power-up;

This study shall result in a Feasibility and Risk analysis Report (FRR), which provides a judgement on the feasibility of the ASIC/FPGA development as defined by the ASIC/FPGA Requirements Specification, as well as an assessment of the risks involved. Every decision taken shall be justified.

5.2.4 ASIC/FPGA development plan

This activity is a management task that is described in this chapter because of schedule reasons. According to the strategy and approaches specified in the ASIC/FPGA Control Plan, a detailed ASIC/FPGA Development Plan (ADP) shall be prepared, documented and maintained.

The purpose of the ADP shall be to allow an assessment of the proposed development strategy. It shall cover all phases of the ASIC/FPGA development and major activities therein. It shall identify the project external interfaces and constraints, the design flow, resources (equipment, software and personnel), the allocation of responsibilities, outputs to be produced and, finally, a schedule with milestones, decision points, type and number of design reviews.

The Development Plan shall include, but not be limited to:

- a. Name of the ASIC/FPGA and its basic function;
- b. References to the Design Documentation and other applicable and reference documents (e.g. internal and external standards, procedures or coding guidelines);
- c. Development team and assignment of major responsibilities;
- d. The baseline FPGA device or ASIC technology;
- e. Companies involved (foundry, subcontractors, suppliers), indicating their assigned tasks, technical and administrative interfaces;
- f. The design flow (design entry, synthesis, simulation, design verification methods, layout generation and verification, production tests, validation);
- g. Specification of a configuration management system according to ECSS-M-40 (Configuration Management);
- h. Versions and platforms of tools to be used, including the foundry/vendor specific tools. The availability of each tool (at the site as well as the dedication to the particular development) shall be explicitly stated;
- i. Baseline approach for verification, radiation hardening, testability, production test (including fault coverage requirements) and design validation;
- j. Split the ASIC/FPGA development into reasonably sized work packages, indicating inputs, tasks to be performed, resources to be employed and outputs to be generated;
- k. Schedule the ASIC/FPGA development, with estimated effort and duration of each work package and the planned dates of milestones and review meetings;
- l. Identification and full description, including formats, of all relevant outputs, deliverable or not, to be produced along the ASIC/FPGA development (documentation, simulation and test results, test boards, test samples, source or generated code/programs) and measures intended to achieve an adequate quality (e.g. HDL coding conformity to an appropriate set of coding rules).

5.2.5 Initial design review

The Definition Phase shall be concluded by the Initial Design Review (IDR) meeting (see quality assurance chapter 6.2), which shall review the documentation generated within this phase in respect to the following items:

- a. Check that the development activity as defined in the ADP is feasible within the limits imposed by the project requirements, resources, schedule and budgetary constraints.
- b. Check that contingency plans exist for all identified open issues/risk items and that the risk analysed can be taken for starting the Architectural Design phase.
- c. Check that ARS and FRR are complete and documented in a level of detail sufficient to proceed with the Architectural Design and all subsequent design work. This shall include but not limited to:
 1. Summary of the system architecture and all foreseen configurations in which the device can be used;
 2. Specify the external devices connected to the chip and their interface protocols;
 3. Bit numbering and naming convention (to be maintained throughout the design flow);
 4. Format of data structures;
 5. Functionality in all nominal operational modes;
 6. Functionality for error handling;
 7. Functionality in all system test modes;
 8. Internal communication protocols;
 9. Signal processing algorithms;
 10. Definitions of programmable memory elements and their state after reset;
 11. Functional partitioning, establishing a high-level block diagram;
 12. Preliminary architectural and HW/SW partitioning, including external and internal memory mapping;
 13. For components providing software programmability, associated software requirements shall be specified;
 14. State and behaviour of I/Os during and after reset and power-up;
 15. State functions explicitly not implemented in the design, in order to avoid potential misunderstandings;
 16. Pin list, including power supply and test pins, if already known. The pin list shall include name, polarity, bus width, interface protocol;
 17. Electrical specifications (maximum ratings, AC, DC and timing diagrams);
 18. Power dissipation estimates for main functional modes;
 19. Operating conditions (supply, temperature, radiation);
 20. Baseline package and pin-out, if already known.

In the case of a satisfactory result of the IDR meeting an authorisation to proceed with the Architectural Design can be given. The MoM of this meeting shall be added to the Management Documentation (see chapter 7.2.4).

5.2.6 Outputs

The outputs of the Definition Phase are:

- a. The Definition Phase Documentation, containing:
 1. ASIC/FPGA Requirements Specification (ARS);
 2. Feasibility and Risk analysis Report (FRR)
- b. ASIC/FPGA Development Plan (ADP)
- c. MoM of IDR

5.3 Architectural design

5.3.1 General

During the Architectural Design phase, the architecture of the chip shall be defined, verified and documented down to the level of basic blocks implementing all intended functions, their interfaces and interactions. Important selections for the implementation of the chip shall be made or confirmed. All definitions and selections made shall seek compliance with the Definition Phase Documentation. Any deviation must be justified in the Architectural Design Review.

The architecture definition and the baseline choices made during the Definition Phase shall be settled, frozen and documented with a level of detail that allows proceeding with the subsequent Detailed Design.

5.3.2 Architecture definition

As a minimum the following tasks shall be performed and documented in an Architecture Definition Report:

- a. Subdivide the chip into its fundamental functions or blocks, identifying and thoroughly documenting their interfaces, functionalities and interactions. The partitioning and definition of the architecture shall go all the way down to the level required to implement technology specific, transistor- or gate-level mapping;
- b. Select suitable algorithms or/and circuit schemes and their parameters to implement the identified functions;
- c. Identify sub-functions, which can be used as an individual block at different locations of the chip or possibly be compiled as a core for other designs;
- d. Identify a suitable clocking and reset scheme assuring correct transitions of data between clock domains and identify asynchronous parts of the design;
- e. Select (if not yet done), IP-cores to be used and/or previously designed units to be re-used in the design. Procure and verify them. This verification can be done by test cases provided by the IP core vendor, by test benches from an independent source, or by newly designed test programs. In some cases, the verification may have been accomplished during prior instantiations of the core. In such case, the former verification work shall be assessed for being sufficient in the actual system environment, eventually bug-fixes and workarounds and/or additional verification shall be performed;
- f. Identify and eventually procure custom cells, to be used in the design, verify the consistency of the different models delivered (simulation models, layout, timing view etc.);
- g. Models required as an input to the subsequent Detailed Design phase (e.g. synthesisable RTL models) shall be generated;
- h. There is no firm requirement for intermediate behavioural simulations, nor for any model being coded in a particular language or a specific level of abstraction. However, the coding of behavioural models of critical functions and algorithms is strongly encouraged, since they frequently are valuable tools for further verification tasks;

The Architecture Definition Report shall include the architecture broken down to the selected blocks, their interfaces, functionality/algorithms and interactions. Even though the chip and its architecture may be completely described in a simulation model (executable specification), a detailed text specification shall be edited.

5.3.3 Verification plan

A Verification Plan shall be established, defining how the functionality and non-functional requirements stated in the Definition Phase Documentation shall be demonstrated at all levels of modelling, starting from the behavioural level down to the gate level. As a minimum the following items shall be considered:

- a. In the case of ASIC developments with complex digital designs, consider a verification by FPGA prototyping or emulation; [A, F]
- b. Consider requirements for code coverage; [A]
- c. Consider requirements for HW-SW interaction, possibly by performing co-simulation;
- d. Consider application of coding rules.

5.3.4 Architecture verification and optimisation

As a minimum, the following activities shall be performed and documented in an Architecture Verification and Optimisation Report:

- a. Verify that the defined architecture meets the requirements by appropriate simulation and analysis techniques;
- b. The models referred to in chapter 5.3.2 item g. above shall be verified according to the Verification Plan. It is recommended, that an independent verification is performed to avoid masking of design errors;
- c. When allocation and connectivity of hard-macro cells can be an issue, a preliminary floorplan shall assure that the foreseen cells are effectively place- and routable within the given constraints; [F]
- d. The feasibility and risks shall be re-assessed;
- e. The architecture shall be optimised in order to satisfy all requirements. For conflicting requirements (such as power consumption vs. speed and performance, pin count vs. package size, complexity vs. die area), a trade-off in the intended goals and the implementation choices shall be established.

5.3.5 Preliminary data sheet

A preliminary Data Sheet shall be produced, to be updated and completed later on at the end of the ASIC/FPGA development (see chapter 7.4.1 for details).

5.3.6 Architectural design review

The Architectural Design phase shall be concluded by the Architectural Design Review (ADR) meeting (see quality assurance chapter 6.2), which shall review the documentation generated within this phase in respect to the following items:

- a. Check that the selected trade-off meets the requirements fixed during the Definition Phase;
- b. Check that preventive measures and/or contingency plans exist for all identified risk items and that the risk analysed can be taken for starting the Detailed Design;
- c. Check that the Architectural Design Documentation (see chapter 7.3.3) together with the documentation of previous development phases is complete and documented in a level of detail sufficient to proceed with the Detailed Design;

- d. Identify, justify and approve discrepancies between the Architectural Design Documentation and the Definition Phase Documentation;
- e. Check that the planned measures, tools, methods and procedures have been applied.

In the case of a satisfactory result of the ADR meeting an authorisation to proceed with the Detailed Design can be given. The MoM of this meeting shall be added to the Management Documentation (see chapter 7.2.4).

5.3.7 Outputs

The outputs of the Architectural Design phase are:

- a. Architecture Definition Report;
- b. Verification Plan;
- c. Architecture Verification and Optimisation Report;
- d. Preliminary Data Sheet;
- e. Design Database, containing:
 - 1. Simulation models;
 - 2. Verification results;
- f. MoM of ADR

5.4 Detailed design

5.4.1 General

During this phase the high-level architectural design is translated into a structural description on the level of elementary cells of the selected technology/library. Additional information is generated for the subsequent development phases, such as layout constraints, floorplanning, production test programs and a detailed pin description.

For digital designs, the above mentioned design description is the associated technology specific, verified gate-level pre-layout netlist, whereas for analog designs, it is a verified sized transistor-level netlist. However, in many analog designs, there may be no separation between circuit design and layout, as influences from layout such as cross talk and matching have to be considered. Circuit and layout are then developed concurrently, and the reviews for Detailed Design and Layout phases may be held together. Also for FPGAs a combined PDR/CDR meeting may be justified. In these cases also the corresponding output reports can be merged together.

The main output of the Detailed Design is a Design Database, which contains, or allows an automatic and repeatable generation of the above-mentioned inputs to the Layout. The scripts required for this generation are an essential part of the Detailed Design, and all these scripts shall be part of the Design Database.

5.4.2 Design entry

During the Design Entry the following tasks have to be performed and documented in a Design Entry report:

- a. Use the agreed design tools as specified in the ADP (Development Plan). Check their maintenance status, consider known bugs, existing patches, preventive and workaround measures;
- b. Implement the specified test concept during design entry and synthesis (scan paths, DFT logic, measurement points, test busses, boundary scan/JTAG etc);
- c. Implement the specified radiation hardening concept by design and during synthesis;
- d. Continuously verify the results by the appropriate methods, as specified in the Verification Plan;
- e. Determine a suitable pin-out and bonding scheme with particular attention to the technical constraints such as power supply(ies) pin definition and bondability issues;
- f. Select buffers according to the I/O requirements defined in the ASIC/FPGA Requirements Specification;
- g. Establish or refine the floorplan; [F]

5.4.3 Netlist generation

In this step, the source description of the design is translated into the netlist, and any other information required for the layout generation, such as floorplan/placement information, constraints for timing driven layout etc. is generated.

Iterations between design entry, netlist and layout generation are required most of the time. However, iterations back to the Architectural Design, by means of changes in the model released during the ADR, should be avoided as much as possible, and require a re-verification of that model.

As a minimum the following tasks shall be performed and documented in a Netlist Generation report:

- a. Consider the required derating factors;
- b. Ensure that the appropriate library cells are used as to fulfil all the requirements collected in the ASIC/FPGA Requirements Specification;
- c. Select or generate appropriate models for parasitics (e.g. wire load models); [F]
- d. Perform a design parameter centring; [D, F]
- e. Ensure that the intended operating (process, voltage, temperature) and environment (radiation) conditions are considered during the translation and verification exercise;
- f. If synthesis tools are used, scripts shall be generated, which allow performing the fully automatic pre-layout netlist generation in a repeatable way. These scripts being part of the inputs to the design, shall also follow the general requirements for documentation, commenting, version control etc.;
- g. Timing constraints, and vendor-specific design rules shall be all taken into account;
- h. Consider over-constraining if appropriate to anticipate parasitic effects;

5.4.4 Netlist verification

As a minimum the following tasks shall be performed and documented in a Netlist Verification Report:

- a. The netlist shall be verified according to the Verification Plan. The verification shall consider estimated data for the layout parasitics and/or delays;

- b. Perform gate level simulations, if possible using the complete test suite from the architectural design, or an equivalent set of methods, such as formal verification and static timing analysis; [A]
- c. Verify key parameters, such as bias voltages/operating point, frequencies, bandwidth, matching, s-parameters, noise, dynamic and linear ranges, shaping times, etc. A functional verification is required, including the interfaces. [D,F]
- d. If a complete simulation of all modes (including test modes) at top level can not be performed (e.g. due to run-time restrictions), a representative subset shall be simulated, and the not simulated cases shall be verified by an extrapolating analysis;
- e. Verify that the specified test concept is implemented through scan paths, DFT logic, measurement points, test busses, etc.;
- f. Verify that the radiation-hardening concept is successfully included in the netlist. Consider e.g. netlist inspection, SEU injection simulations;
- g. Verify that the specified power consumption is respected;
- h. Update relevant parameters in the preliminary Data Sheet according to the results obtained during the verification;
- i. If production tests or a pre- and post burn-in test are foreseen, generate the test vectors and verify the requirements for fault coverage;
- j. For IP cores and macro cells: include the core's test patterns in the overall ASIC's test programmes;
- k. Verify, that the pre-layout vendor design rules are met and assess the relevance of violations; [F]
- l. Perform a parameter sensitivity analysis; [D, F]

5.4.5 Updated data sheet

The Data Sheet shall be updated to incorporate the new established information on pinout, estimated timing, etc. For further details see chapter 7.4.1.

5.4.6 Preliminary design review

The Detailed Design phase shall be concluded by the Preliminary Design Review (PDR) meeting (see quality assurance chapter 6.2), which shall review the documentation generated within this phase in respect to the following items:

- a. Check that the Detailed Design Documentation (see chapter 7.3.4) together with the documentation of previous development phases completely documents all results obtained and decisions made along with the corresponding justifications in a level of detail sufficient to proceed with the Layout. This shall include but not limited to:
 - 1. Circuit implementation: Describes details of the implementation, which were not specified during Architectural Design;
 - 2. Description of implemented testability and production test methods including the achieved fault coverage figures obtained;
 - 3. Description of implemented radiation hardening measures;
 - 4. All verification results;
 - 5. Description of cells specially developed for the design;

6. Configuration and modifications applied to IP cores used in the design;
 7. List of items with name and format provided to the foundry (i.e. netlist, stimuli files for production test, constraints files etc.); **[F]**
 8. The design database shall be fully described, including the file structure, naming conventions, version control labels, netlist generation methods and constraints;
 9. All tools and ASIC libraries actually used during the entire design development shall be documented, including the versions and operating platforms used;
 10. Problems encountered with design tools and their workarounds;
- b. Check that the planned measures, tools, methods and procedures have been applied;
 - c. Check that the outputs are compliant with the requirements fixed during the Definition Phase;
 - d. In particular, when the layout is performed by another company (foundry), specific foundry requirements (netlist sign-off criteria) must be assessed;

In the case of a satisfactory result of the PDR meeting an authorisation to proceed with the Layout can be given. The MoM of this meeting shall be added to the Management Documentation (see chapter 7.2.4).

5.4.7 Outputs

The outputs of the Detailed Design phase are:

- a. Design Entry Report;
- b. Netlist Generation Report;
- c. Netlist Verification Report;
- d. Updated Data Sheet with pin-out;
- e. Updated Design Database, containing:
 1. Pre-layout netlist;
 2. Constraints for layout (floorplan, constraints for timing driven layout, etc.) as defined in the ADP;
 3. Test vectors for production test;
- f. MoM of PDR

5.5 Layout

5.5.1 General

The layout shall generate the placement and routing information to meet the design rules, timing and other constraints. If Detailed Design and Layout phases are combined, netlist optimisation by local re-synthesis may be applied. This phase provides reliable information about loads and coupling capacitors and the final design rule check that assures a verified netlist which can be forwarded to the foundry.

5.5.2 Layout generation

As a minimum the following tasks shall be performed and documented in a Layout Generation Report:

- a. Finalise the floorplan of the chip; [F]
- b. Perform Place & Route (P&R) taking into account all layout constraints;
- c. Perform netlist optimisations (see chapter 5.5.1) for timing and design rules if necessary; [F,A]
- d. Generate the power distribution;
- e. Generate the clock distribution (clock tree and buffers); [A]
- f. Insert core and pad ring power distribution and possibly additional test pads in the circuit;
- g. Determine the die size; [F]
- h. Generate the bonding diagram respecting bonding and package constraints; [F]
- i. Generate the Input Data for Mask or Programming file generation (IDMP).

5.5.3 Layout verification

As a minimum the following tasks shall be performed and documented in a Layout Verification Report:

- a. Layout Design Rule Check (DRC);
- b. Electrical Rule Check (ERC), check cross-talk sensitivity, if required by customer;
- c. Extract a netlist from the layout given in terms of IDMP;
- d. Verify that the post-layout netlist is consistent with the layout representing IDMP by performing a Layout Versus Schematic (LVS) comparison, or by performing a Netlist Comparison Check (NCC) between the post-layout netlist and the layout (IDMP) extracted netlist;
- e. Verify that the post-layout netlist is consistent in terms of functionality with the pre-layout netlist by simulation and formal methods;
- f. Extract the parasitic information. This delivers capacitance, resistance and inductivity values (only deep sub-micron technology), from which the actual delays are calculated for digital designs;
- g. Perform comprehensive post-layout verification according to the Verification Plan. This is mostly accomplished by back-annotated simulations and timing analysis;
- h. Check the resulting clock skew and latency; [F]
- i. Check relevant timing of I/Os;
- j. Check the power distribution on the chip; [F]
- k. Perform transition check and load check on the nets inside the ASIC;
- l. ASIC/FPGA performances shall be characterised, such as max clock frequency, clock duty cycle, set-up and hold times for all inputs, propagation delays for all outputs

5.5.4 Design validation plan

This activity is a management task that is described in this chapter because of schedule reasons. The purpose of the Design Validation Plan (DVP) shall be to specify the measurements that shall be performed on the prototypes in order to verify that the new implemented devices contain the functionality and the characteristic they are designed for. According to the approaches specified in the ADP (see chapter 5.2.4), the DVP shall include but not limited to:

- a. description and requirements for an appropriate test set-up or system breadboard;
- b. operating modes and test conditions of the prototypes under test;
- c. characteristics and functions to be validated and checked against the ASIC/FPGA Requirements Specification
- d. if a radiation test is required by the customer, the corresponding radiation verification plan shall be established.

5.5.5 Updated data sheet

Update relevant parameters in the Data Sheet according to the results obtained during the layout verification. For further details see chapter 7.4.1.

5.5.6 Draft detail specification

Based on the information collected in the Design Documentation a draft Detail Specification shall be established according to the requirements given in chapter 7.4.3.

5.5.7 Critical design review

The Layout phase shall be concluded by the Critical Design Review (CDR) meeting (see quality assurance chapter 6.2), which shall review the documentation generated within this phase in respect to the following items:

- a. Check that the Layout Documentation (see chapter 7.3.5) together with the documentation of previous development phases completely documents the progress and decisions made during the Layout. As a minimum it shall include:
 1. Post-layout clock distribution tree and clock skew and latency analysis;
 2. Post-layout verification results and analysis of timing margins;
 3. Results from all layout checks (e.g., DRC, ERC, LVS/NCC etc.) Any violation of or deviations from the design rules shall be documented and justified.
- b. Check that the planned measures, tools, methods and procedures have been applied;
- c. Check that the outputs are compliant with the requirements fixed during the Definition Phase;
- d. In the case where no PDR was held after the Detailed Design phase, check that the CDR encompasses also all review items of the PDR;
- e. Check that preventive measures and/or contingency plans exist for all identified risk items and that the risk analysed can be taken for starting the Prototype Implementation;

After a satisfactory result of the CDR meeting, the production release (tape-out) can be given. The MoM of this meeting shall be added to the Management Documentation (see chapter 7.2.4).

5.5.8 Outputs

The outputs of the Layout phase are:

- a. Layout Generation Report;
- b. Layout Verification Report;
- c. Design Validation Plan
- d. Updated Data Sheet;
- e. Draft Detail Specification;
- f. Updated Design Database, containing:
 1. Post-layout netlist in the agreed format depending on the targeted technological approach (GDS II, FPGA P&R files or other);
 2. Corresponding parasitic information;
- g. MoM of CDR

5.6 Prototype implementation

5.6.1 General

In this phase chips are manufactured and packaged, or FPGA's programmed, and the prototypes are tested. In the following, the term production or implementation refers to chip manufacturing/packaging, or FPGA programming, whatever is applicable. The phase is concluded by the delivery of the tested devices.

5.6.2 Manufacture/programming and test

As a minimum, the following tasks shall be performed and documented in a Production Test Report:

- a. The package shall be the same as for flight devices, if required by the customer;
- b. The mask generation and verification shall be performed under the foundry's configuration control system; **[F]**
- c. The committed number of prototypes shall be produced and delivered, so that design validation can be performed;
- d. The production test shall be performed on 100 % of the delivered prototypes, using the test vectors generated during the previous phases. The production test shall demonstrate, that the device was produced correctly. **[F]**
- e. The correctness of the FPGA programming shall be verified (checksum test). **[D, A]**
- f. The tested parameters and conditions shall be according to the draft Detail Specification (see chapter 7.4.3);
- g. Test reports shall be generated and delivered, documenting the measured parameters. Tester log files shall be delivered in electronic format;

5.6.3 Outputs

The generated outputs of the Prototype Implementation phase are:

- a. Agreed number of tested devices (ASICs or FPGAs);

ECSS-Q-60-02

- b. Production test results and reports; **[F]**
- c. Burn-in or any other production test results, specifications and patterns;

5.7 Design validation and release

5.7.1 Design validation

The design validation shall be performed to confirm the achievement of all functional, performance, interface and compatibility requirements.

As a minimum, the following tasks shall be performed and documented in a Validation Report:

- a. The validation shall be carried out according the established Validation Plan;
- b. An appropriate test set-up or system breadboard shall be designed and built to represent a realistic system application;
- c. This breadboard shall be employed to perform validation tests that cover full functionality and all operating modes and conditions of the device;
- d. If contractually agreed, specific burn-in or other screening tests shall be established for the later test of the FM parts;
- e. Scope, sequences, set-up and results of the validation tests shall be documented in the Validation Report which shall become part of the Design Validation Documentation. Specified parameters shall be compared with measured parameters. The Validation Report shall be made available to the foundry and the design house.

5.7.2 Radiation test performance

The device prototypes shall undergo radiation testing according to the requirements of the project, if the required hardening level is not yet demonstrated for the technology involved. This activity shall be performed according to the established radiation verification plan included in the Design Validation Plan and documented in a Radiation Test Report.

5.7.3 Design release and FM production preparation

For the design release and FM production preparation, the following requirements shall be fulfilled and documented in a Release Report:

- a. License agreements for the intellectual property (the design itself and 3rd party IP cores) contained in the device shall be established to cover the whole lifetime;
- b. Technical support of the device shall be assured during the lifetime of the product. This can be accomplished through a know-how transfer from the design house to the foundry or a third party, or by the design house itself;
- c. The storage of the complete design database shall be assured during the lifetime of the product, including associated data, documentation, pattern generation files, test program(s) and mask sets used;
- d. In the case of using non-QML manufacturer/foundry, an evaluation programme (see ECSS-Q-60) has to be performed that include as agreed by the customer the following activities:
 - manufacturer evaluation;
 - constructional analysis;
 - evaluation testing.On completion of the evaluation programme sufficient additional data such as reliability and radiation data shall be available that ensures that the mission requirements can be met.
- e. Assessment of the risk involved for the FM production.

5.7.4 Experience summary report

This activity is a management task that is described in this chapter because of schedule reasons. The purpose of the Experience Summary Report shall be to collect the experience gained during the execution of the ASIC/FPGA procurement programme as detailed in chapter 4.3.

5.7.5 Final versions of application and procurement documents

The Detail Specification (see chapter 7.4.3) and, if requested by the customer, the Data Sheet (see chapter 7.4.1) shall be updated based on the validation test results. The Data Sheet, eventually transformed to the foundry specific format, shall be available during the device lifetime.

If requested by the customer an Application Note (see chapter 7.4.2) shall be established.

5.7.6 Design validation review

The Design Validation phase shall be concluded by the Design Validation Review (DVR) meeting (see quality assurance chapter 6.2), which shall review the documentation generated within this phase in respect to the following items:

- a. Check that the Design Validation Documentation (see chapter 7.3.6) together with the documentation of previous development phases is complete;
- b. Check that the device has achieved functional, performance, interface and compatibility characteristics satisfying the ASIC/FPGA Requirements Specification;
- c. Check that the planned measures, tools, methods and procedures have been applied;
- d. Check that preventive measures and/or contingency plans exist for all identified risk items and that the risk of FM production can be taken.

With the successful completion of the DVR meeting the new developed ASIC or programmed FPGA can be released for FM production. The MoM of this meeting shall be added to the Management Documentation (see chapter 7.2.4).

5.7.7 Outputs

The outputs of the design validation and release phase are:

- a. Validation Report
- b. Radiation Test Report (if applicable)
- c. Release Report
- d. Experience Summary Report
- e. Final Data Sheet
- f. Final Detail Specification
- g. Application Note
- h. MoM of DVR
- i. Validation Breadboard
- j. Burn-in or Screening Test Boards for FM parts

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6. Quality assurance system

6.1 General

The quality assurance requirements defined in ECSS-Q-20 subclause 4.4 (QA status reporting), ECSS-Q-30 subclause 6.4 (Criticality classification of functions and products) and ECSS-Q-60 subclause 4 (Components quality assurance) shall apply. It shall be the objective of the quality assurance system to ensure the development of reliable, manufacturable, testable and reproducible, custom designed components for space application.

The tools to be used shall be specified in the contract. All technology independent CAD tools to be employed during the development shall be mature and fit for their purpose. All technology dependant CAD tools shall be used as approved and supported by the selected manufacturer. Preference shall be given to the use of established international standards, such as VHDL as defined in IEEE 1076 and EDIF.

For custom designed devices with long term availability or multiple usage requirements prospective design portability shall be maximised as economically feasible. This shall include both design and manufacturing. Factors to be taken into account shall include but not be restricted to:

- a. alternative technologies and manufacturers;
- b. package and die size compatibility;
- c. compatibility of CAD tools;
- d. effort/cost of design portation;
- e. interchangeability of processes and cell libraries;
- f. test pattern files and description (high level language);
- g. simulation approach (hierarchical, block oriented);
- h. safe keeping of intermediate design files.

6.2 Review meetings

The supplier shall be responsible for the scheduling and conductance of design reviews. They shall be defined along with the criteria for their successful completion in the ASIC/FPGA Development Plan (see chapter 5.2.4). Suitable representation, for design and quality assurance, from all relevant organisations (customer, system contractor, design house and foundry) shall be ensured.

The supplier shall produce and circulate in advance of each design review a design review package containing a checklist based on the established requirements and the data necessary for the particular review.

The completion of the following design reviews is mandatory:

a. **Initial Design Review (IDR)**

This review shall result in the authorisation to start the Architectural Design. As a minimum it shall approve the consistency, quality, feasibility and risk assessment of the Definition Phase Documentation. The outputs to be reviewed and the items to be checked are detailed in chapter 5.2.5;

- b. **Architectural Design Review (ADR)**
This review shall result in the authorisation to start with the Detailed Design. It shall identify, justify and approve discrepancies between the Architectural Design and the Definition Phase Documentation. It shall identify the preferred technology and check that the contingency plan was updated. The outputs to be reviewed and the items to be checked are detailed in chapter 5.3.6;
- c. **Preliminary Design Review (PDR)** (if applicable)
This review shall result in the authorisation to proceed with the Layout. As a minimum it shall cover and approve the design decisions/trade-offs taken during the Detailed Design phase (acc. to chapter 5.4), the conformance to reliability, testability and radiation hardening requirements, and the extend and results from simulations in this phase. The risk mitigation activities shall be checked. The outputs to be reviewed and the items to be checked are detailed in chapter 5.4.6.
In the case the design and layout is a concurrent or interdigitated activity (typical for analog or FPGA design) this review meeting can be combined with the subsequent CDR meeting;
- d. **Critical Design Review (CDR)**
This review shall result in the approval of design and layout and the release for prototype implementation. As a minimum it shall cover and approve the layout, final simulations (acc. to chapter 5.5) and the production test, the Design Validation Plan and the risk mitigation activities. The outputs to be reviewed and the items to be checked are detailed in chapter 5.5.7. Direct or delegated customer participation and manufacturer / foundry participation is mandatory.
- e. **Design Validation Review (DVR)**
This review shall result in the final acceptance of the design. As a minimum it shall cover and approve the production test and design validation test results and all documentation produced and updated in this phase. The outputs to be reviewed and the items to be checked are detailed in chapter 5.7.6. Direct or delegated customer participation shall be mandatory.
- f. Additional design reviews shall be performed as needed.

The decision on a satisfactory result of a review meeting can only be achieved by a consent of all parties. A review identifying a limited number of only minor discrepancies can be completed after successful implementation of the corrective actions defined during the review.

A review failing major acceptance criteria and resulting in a design iteration shall be repeated in full.

The criteria for a successful review meeting shall be defined prior to the relevant meeting. It is recommended to define these criteria on the preceding review meeting.

All review meetings shall be minuted.

6.3 Risk assessment and risk management

The design risk for the timely and successful completion of the development activity shall be assessed according to the items listed in para 5.2.3.2. This activity shall be done concurrently to the design activity.

Extraordinary risks shall be covered by a contingency plan identifying alternative or back-up solutions.

A check of the risk mitigation activities shall be a major item of the agenda of every review meeting.

6.4 Supplier dependability

Actors involved in the ASIC/FPGA development such as foundry, subcontractors, service providers and other shall be obliged by contractual agreements to respect the following as a minimum:

- a. All activities shall be compliant to the requirements of this document;
- b. The property rights of the individual parties involved in the ASIC/FPGA development shall be kept;
- c. All parties commit to keep confidential specifications and results of the development activity and not to forward any information to third parties for a period of the expected lifetime of the device;

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7. Development documentation

7.1 General

At all stages of the ASIC/FPGA development the supplier shall be responsible for the production, maintenance, control and archiving of all related documentation as defined and detailed in the following paragraphs.

All documentation shall be in English. The documentation shall be well structured and easily readable, so that the design can be understood by an ASIC/FPGA designer internal of the supplier/manufacturer not being involved in the design work. Names of signals, blocks etc. shall be chosen to indicate their function, and shall be based on English. The documentation shall be consistent, e.g. the same item shall have the same name in all documentation. Block diagrams, control flow charts, timing diagrams and other figures shall be introduced where beneficial for the understanding of the text. Every time an updated document is delivered it shall include a detailed change list, and all significant changes marked using a change bar in the margin. If a document is delivered before being complete, each page with incomplete information shall be clearly marked. Some of the information listed is normally better delivered separately or in appendices, such as layout plots, gate-level schematics, lists of undetected faults etc.

All documents shall be archived for a minimum period of five years after completion of the development activity or as agreed by the customer.

The development documentation shall be structured in order to reflect and record the concurrent development activities on the management and engineering level that shall result in the establishment of the required application and procurement documents for the implemented devices.

7.2 Management documentation

7.2.1 General

The management documentation shall provide the overall strategy for the development activity including task planning and organisation and approaches, methods and procedures that shall be applied. It also includes the status reporting as MoM of the review meetings and an assessment of the experience gained during the development activity. The management documentation is a gathering of separate documents.

7.2.2 ASIC/FPGA control plan

The purpose of the ASIC/FPGA Control Plan (ACP) shall be to specify the organisation, management tools, strategy, approaches and procedures that shall be adopted to accomplish the intended ASIC/FPGA development. The ASIC/FPGA Control Plan is detailed in chapter 4.2.

7.2.3 ASIC/FPGA development plan

The purpose of the ASIC/FPGA Development Plan (ADP) shall be to allow an assessment of the proposed development strategy. It shall cover all phases of the ASIC/FPGA development and major activities therein. A detailed list of items, the ADP shall address, is given in chapter 5.2.4.

7.2.4 Minutes of review meetings

The minutes of the review meetings (see chapter 6.2) shall describe the status of the project by listing the requirements fulfilled for the reviewed development stage. For requirements not fulfilled actions shall be defined and due dates for their completion shall be fixed.

For a satisfactory review meeting the minutes shall contain the agreement on an authorisation to proceed with the next stage of the ASIC/FPGA development.

The minutes of the review meetings shall become appendices of the development plan.

7.2.5 Verification plan

The Verification Plan shall define the methods to be used to verify the correct implementation of the functionality and non-functional requirements stated in the Definition Phase Documentation as detailed in chapter 5.3.3.

7.2.6 Design validation plan

The purpose of the Design Validation Plan (DVP) shall be to specify measurements that shall be performed on prototypes in order to verify that the new implemented devices contain the functionality and the characteristic they are designed for. The DVP shall include the description and requirements for an appropriate test set-up or system breadboard and the operating modes and test conditions of the prototypes as detailed in chapter 5.5.4.

7.2.7 Experience summary report

In the frame of the supplier's continued quality improvement activities and to establish economic and efficient development and test requirements for expected future projects, the supplier should collect and evaluate continuously, and present in an experience summary report any relevant information as detailed in chapter 4.4 resulting from the experience gained during the execution of the ASIC/FPGA procurement programme.

7.3 Design documentation

7.3.1 General

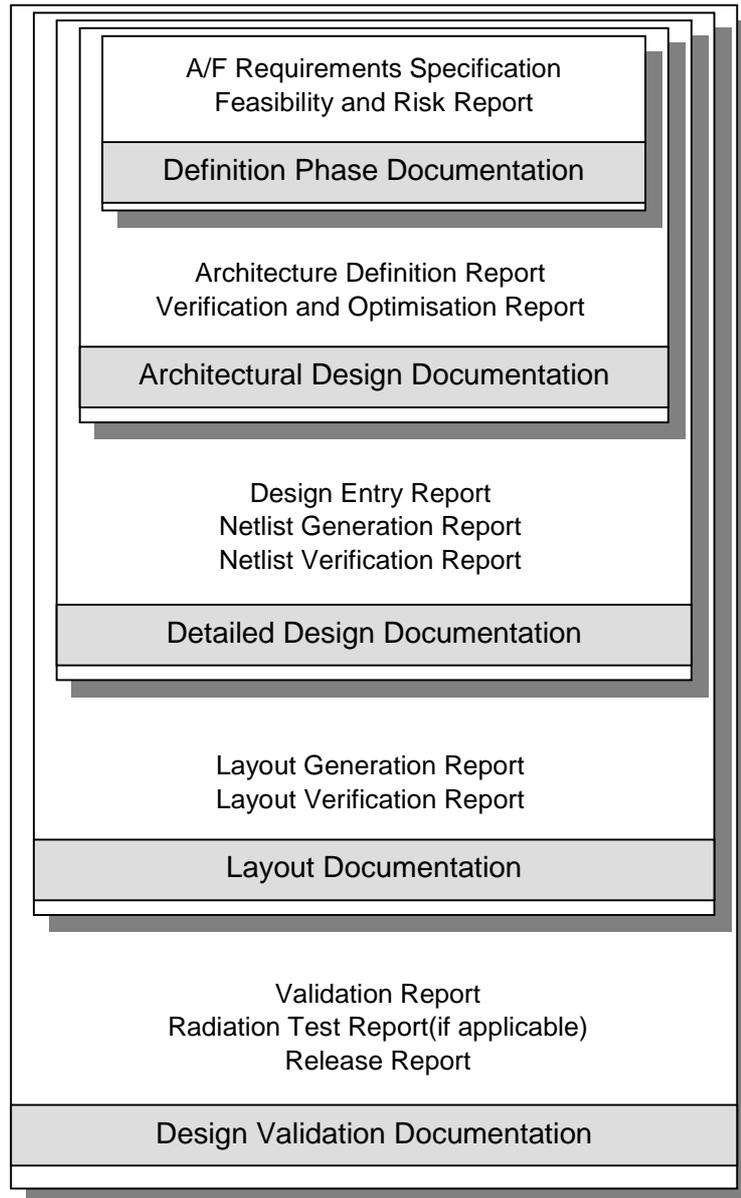
The purpose of the Design Documentation (DD) shall be to record the progress achieved and the decisions made along with the corresponding justifications during the development phases of the device.

All design information shall be stored in a design database by applying the contractual agreed revision control mechanism (see chapter 5.1). All intermediate design data shall be reproducible to assist possible iterations. As the design database consists of electronic data that cannot be reviewed directly, reports shall be established that need not to have a document format but contain a legible extract of the database. The reports that shall be produced during the individual phases of a typical development activity are detailed in the following chapters. An example of a suitable filing of this Design Documentation is given in chart II.

In the case the design and layout is a concurrent or interdigitated activity (typical for analog and FPGA design) the corresponding output reports can be merged together.

Chart II

Design Documentation



7.3.2 Definition phase documentation

The Definition Phase Documentation consists of the following contributions:

- a. **ASIC/FPGA Requirements Specification (ARS)**
The ARS shall be established during the first development phase and shall include a complete set of ASIC/FPGA requirements, as detailed in chapter 5.2.2, that are settled, unambiguous and frozen.
- b. **Feasibility and Risk analysis Report (FRR)**
The FRR is the second part of the Definition Phase Documentation and shall give a judgement on the consistency and quality of the ASIC/FPGA and system requirements and the feasibility of the ASIC/FPGA development as well as an estimate of the risk involved. It shall cover the items detailed in chapter 5.2.3.

7.3.3 Architectural design documentation

The Architectural Design Documentation adds the following contributions to the Definition Phase Documentation:

- a. **Architectural Definition Report**
The Architecture Definition Report shall include the architecture broken down to the selected blocks, their interfaces, functionality/algorithms and interactions as specified in chapter 5.3.2.
- b. **Verification and Optimisation Report**
The Verification and Optimisation Report shall document the simulations performed and the results received and the implementation choices and trade-offs found to optimise the architecture. Further details are given in chapter 5.3.4.

7.3.4 Detailed design documentation

The Detailed Design Documentation adds the following contributions to the Architectural Design Documentation:

- a. **Design Entry Report**
The Design Entry Report shall document all inputs available for the Detailed Design phase as detailed in chapter 5.4.2.
- b. **Netlist Generation Report**
The Netlist Generation Report shall describe the work performed and the decisions taken to generate a netlist as detailed in chapter 5.4.3.
- c. **Netlist Verification Report**
The Netlist Verification Report shall list all steps of simulation and verification performed (see chapter 5.4.4) together with the corresponding results.

7.3.5 Layout documentation

The Layout Documentation adds the following contributions to the Detailed Design Documentation:

a. **Layout Generation Report**

The Layout Generation Report shall describe the work performed and the decisions taken to generate layout as detailed in chapter 5.5.2.

b. **Layout Verification Report**

The Layout Verification Report shall list all steps of verification performed (see chapter 5.5.3) together with the corresponding results.

7.3.6 Design validation documentation

The Design Validation Documentation adds the following contributions to the Layout Documentation:

a. **Validation Report**

The Validation Report shall present the scope, sequences, set-up and results of the validation tests performed as detailed in chapter 5.7.1.

b. **Radiation Report** (if applicable)

The Radiation Report shall document the test board circuitry and bias conditions, the test sequence and investigated irradiation levels, the performed measurements and the resulting degradations.

c. **Release Report**

The Release Report shall summarise all activities performed to assure that all necessary prerequisites are fulfilled to start a FM production (see chapter 5.7.3).

7.4 Application and procurement documents

7.4.1 Data sheet

If requested by the customer, a Data Sheet shall be established that describes the functionality of the device so it can be used by a board or system designer.

Each page shall contain the device name and number and the date of issue. The first page should contain a summary of the device functionality, a block diagram and short list of features, such as operating frequency, technology etc., and the foundry address.

All characteristics and limitations introduced during the design shall be described, such as detailed interface descriptions, register definitions, memory maps etc.

The Data Sheet shall include a system overview of the device and a description of how to use the device in a typical system, including an application block diagram.

The full functionality and all operating modes shall be specified in detail.

All signal interfaces shall be described in detail including description of all signals, test and power pins etc., specifying the usage of the signals, the signal polarity etc. The signal descriptions shall be grouped according to their function.

All electrical and mechanical data shall be specified, together with their relevant applicable conditions (temperature, capacitive load etc.), including:

- a. Absolute maximum ratings, including storage temperature, operating temperature, supply voltage, maximum input current for any pin, total dose, Single Event Upset, latch-up, electrostatic discharge and reliability figures;
- b. DC parameters, including voltage levels, leakage currents, pin capacitances and output currents;
- c. Static and dynamic (per MHz) power dissipation, allowing the power consumption at lower operating frequencies to be calculated, if representative;
- d. AC parameters, including set-up and hold times, cycle periods, output delays, tri-state delays etc., together with waveform diagrams. The timing parameters shall be related to the relevant reference signal edges;
- e. Package description, including pin assignment, package figure with pin numbers and preferably signal names, and a mechanical drawing for the package dimensions including information on the thermal characteristic of the package such as wall thickness, thermal coefficient of material and/or package.

A preliminary data sheet shall contain all parts of a final data sheet, with the same level of detail. Where data is not known, estimates shall be used and clearly indicated to be estimates.

7.4.2 Application note

If requested by the customer, an Application Note shall be established for components which are regarded as standard parts for a variety of system applications. In such a case the application note shall guide the user through the possible configurations the device/module can be operated with. Typical examples for the corresponding bias circuitry, supply voltages and configuration signals shall be provided.

7.4.3 Detail specification

All devices intended for use as FM products shall be procured according to controlled specifications. All new specifications shall be designed to be totally compliant with one of the existing European standardisation systems. New Detail Specifications shall include the following as a minimum:

- a. Relevant electrical and mechanical parameters;
- b. Screening, burn-in, and acceptance requirements;
- c. Deviations from the generic specification;
- d. Documentation / data requirements;
- e. Delta limits, when applicable;
- f. Criteria for percent defective allowable;
- g. Lot Acceptance Tests / Quality Conformance Inspections;
- h. Marking;
- i. Storage Requirements;
- j. Requirements for lot homogeneity;
- k. Serialisation, when applicable;
- l. Protective packaging and handling requirements;
- m. Radiation Verification Testing requirements, when applicable;

Specifications shall include configuration control requirements that ensure that any change of the product that refers to the qualification or that may affect performance, quality, reliability and interchangeability is identified by the manufacturers.

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8. Deliverables

8.1 General

- a. Upon request, the customer shall receive free of charge from the manufacturer / foundry, for the duration of the development, a complete design kit for the selected process, including all libraries and design kit tools and their complete documentation, in order to allow the customer to independently verify the design. This only applies if such a design kit actually exists for the design tools available at the customer;
- b. The quantity to be delivered of each individual deliverable item shall be agreed between customer and supplier according to the requirements of the actual project. Additional items shall be defined as necessary;
- c. Each delivery of a design document shall be accompanied by a written statement of the status of the deliverable item. The IP rights have to be considered;
- d. Paper copies shall be easily readable and suitable for subsequent photo-copying. Electronic copies shall be submitted on in an agreed format via electronic media;
- e. Text files shall be in Adobe Acrobat Reader, Frame Maker or ASCII format (for documents ASCII only after customer agreement);
- f. Photos and layout plots may be part of the documentation only for promotional information with restricted details, if not specified elsewhere;

8.2 Deliverable items

The list of deliverables will be defined per contractual agreed SOW. Table 1 presents all documentation, software and hardware deliverables that become available during the ASIC/FPGA development. These deliverables shall be considered during negotiations between Customer and Supplier.

Table 1 Deliverables of the ASIC/FPGA Development

Development Phase	Documentation	SW	HW
	A/F Control Plan		
Definition Phase	A/F Requirements Specification Feasibility and Risk Report A/F Development Plan MoM of IDR		
Architectural Design	Architecture Definition Report Verification Plan Architecture Verification and Optimisation Report Preliminary Data Sheet MoM of ADR	Design Database containing: Simulation models Verification Results	
Detailed Design	Design Entry Report Netlist Generation Report Netlist Verification Report Updated Data Sheet MoM of PDR	Updated Design Database containing: Pre-layout netlist Constraints for layout Test vectors for production	
Layout	Layout Generation Report Layout Verification Report Design Validation Plan Updated Data Sheet Draft Detail Specification MoM of CDR	Updated Design Database containing: Post-layout netlist Corresponding parasitic information	
Prototype Implementation	Production Test Results and Reports Burn-in or any other production test results, specification, pattern		Agreed number of Tested Devices (ASICs or FPGAs)
Design Validation and Release	Validation Report Radiation Test Report Release Report Final Data Sheet Final Detail Specification Application Note Experience Summary Report MoM of DVR		Validation Breadboard Burn-in or Screening Test Boards for FM parts

8.3 Acceptance of deliverable items

Provisional acceptance is given upon reception and brief review of each deliverable item. Final acceptance is given within a period contractually agreed in the SOW, if no discrepancies are found between the specifications - including agreed changes - and the delivered items.

If a design is delivered without subsequent manufacturing, it is accepted upon approval of the database and documentation.

Annex A

Informative references

The following references have been used during the preparation of this document:

ASIC/001	VHDL Modelling Guidelines, Issue 1, September 1994
JPL	The NASA ASIC Guide, Draft 06, 1993
QC/172/RdM	ESA ASIC Design and Assurance Requirements, Issue 1, June 1992
WDN/PS/700	ASIC Design and Manufacturing Requirements, Issue 2, October 1994
MIL-STD-883	Test Method Standard Microcircuit
IEEE 1076	Very High Speed Integrated Circuit Hardware Description Language
IEEE 1149.1	Boundary Scan (JTAG) Interface