Design, Simulation and Hardware Implementation of a Digital Television System: Synchronization Techniques

(Invited Paper)

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Abstract—As described in [1], in 2005 the Brazilian government supported many research consortia in order to develop a Digital Television System employing advanced technologies for multimedia broadcasting. One of the proposals for the physical layer of this system was entitled Innovative Modulation for the Brazilian Digital TV System (MI-SBTVD). The MI-SBTVD Project includes high performance error-correcting codes, transmit spatial diversity and multi-carrier modulation. The objective of this article is to present the synchronization techniques that were used in the first proof-of-concept for the MI-SBTVD System. We present the simulated performance results for both the AWGN and multipath channels. Finally, we also comment on the implementation details of the synchronization scheme using Field Programmable Gate Array (FPGA) devices.

Keywords - OFDM Synchronization, Digital Television, SBTVD.

I. INTRODUCTION

Since the 80’s the transition from analog to digital TV has been discussed and implemented in different countries. Basically, there are three standards that dispute the international scenario. They are the American ATSC [2], the European DVB [3], and the Japanese ISDB-T standard [4]. These three systems make use of the same video compression technology, namely, the MPEG-2. On the other hand, they differ with respect to the modulation and channel coding techniques.

The ATSC standard is based on a single carrier system with 8-VSB modulation [5], while DVB and ISDB-T are based on an OFDM (Orthogonal Frequency Division Multiplexing) transmission [6] with various QAM modulation levels. Since these standards have been developed with technologies of the 90’s, there is room enough for improvements. In the year 2005 the Brazilian government contracted twenty consortia, composed by a large number of researchers, to initiate the development of a Brazilian Digital Television System (SBTVD). The development should incorporate the state of the art techniques which could provide considerable gains over the older standards.

The MI-SBTVD consortium was composed by the National Institute of Telecommunications (INATEL), the State University of Santa Catarina (UFSC), the Federal University of Campinas (UNICAMP), and the Federal Technological University of Paraná (UTFPR) and by Linear Equipments Co. The MI-SBTVD Project uses LDPC channel coding and a modulation system that combines OFDM and space-time codes (STC) [7]. Such a STC-OFDM system [8] is a very efficient technique for situations where high data rates must be transmitted over a multipath channel, under both static and mobile scenarios.

In order to guarantee correct demodulation at the receiver, the system needs to compensate for the propagation delays, Doppler effects and oscillator imperfections. This can be achieved by the use of a properly designed synchronization technique, which plays a major role on the system performance, especially in OFDM systems [9] [10]. The transmitter and receiver for the proposed STC-OFDM system are shown in Figures 1 and 2, respectively. It is important to emphasize that the conventional synchronization techniques for single transmit antenna OFDM systems may not work in a STC-OFDM system. Particular characteristics of the STC-OFDM modulation must be taken into account for the proper design of the corresponding synchronization schemes.

The primary objective of the present paper is to present the details of the synchronization scheme for the proposed digital television system. Theoretical aspects and practical hardware implementation issues are also presented. Some interesting results for AWGN and multipath channels are emphasized.
II. SYNCHRONIZATION FOR OFDM RECEIVERS WITH SPACE-TIME CODES

Synchronism is one of the most important parts of an OFDM receiver. It is an indispensable process that is used to compensate for the presence of system imperfections, such as oscillator offsets, Doppler Effects and propagation delays.

Let us call \( f_{\text{error}} \) the frequency offset between the transmitter and the receiver, \( \theta \) the phase offset and \( \tau_{\text{error}} \) the timing offset at the receiver. These parameters allow us to describe the received signal \( r(t) \) as

\[
r(t) = s(t - \tau) e^{j2\pi f_{\text{error}}t + \theta} + n(t),
\]

where \( s(t) \) is the transmitted signal and \( n(t) \) is a white and Gaussian noise added by the channel. In this paper we are not interested in phase synchronization, since this can be easily accomplished by the channel equalizer without any loss in performance. Therefore, henceforth we will not take into account the phase \( \theta \) in our equations.

As shown in [9] and [10], it is possible to observe that the carrier frequency offset causes ICI (Inter-Carrier Interference) in the received signal. If the timing offset is not compensated for and if it is larger than the cyclic prefix, \( T_{CP} \), then ICI and ISI (Inter-Symbol Interference) will arise [9] [10].

The synchronization techniques can be divided into two categories, namely, the blind (non-pilot aided) [11]-[13] and the supervised synchronization (pilot-aided). In the latter the receiver has a priori knowledge of some of the transmitted signals, which can be multiplexed in time or in frequency domain [14]-[16]. In the specific case of the blind techniques, some algorithms for them explore some correlation properties induced by the cyclic prefix insertion.

As presented in Figure 1 and according to [9] and [10], the synchronism process can be divided into two parts, namely, the Carrier Frequency Offset (CFO) synchronization, which corrects the \( f_{\text{error}} \), and the FFT (Fast Fourier Transform) Window Timing (FFT-WT) synchronization, which accounts for the timing offset \( \tau_{\text{error}} \). Usually, the CFO needs a timing reference, obtained by the DFT-WT technique, in order to extract the \( f_{\text{error}} \) parameter, as shown in Figure 2.

Time and frequency synchronization can be achieved in two stages, the coarse and the fine synchronization phases. While coarse synchronization is achieved in the time domain, usually in the acquisition phase, fine synchronization can be achieved in frequency domain [10]. The latter is used to track or refine the synchronization parameters.

A. Losses Caused by Synchronization Errors

Large values of \( f_{\text{error}} \) increase ICI and large values of \( \tau_{\text{error}} \) increase ISI as well, resulting in performance degradation. According to [10], it is possible to describe the performance degradation on AWGN channels, in terms of the SNR (Signal to Noise Ratio), as a function of \( f_{\text{error}} \) and \( \tau_{\text{error}} \), which is given by the following equations

\[
SNR_m \approx \frac{E_s (m) \sin^2 (f_{\text{error}} T_S)}{N_0 + E_s (m) \sum_{n=0, n \neq m}^{N-1} \sin^2 (n - m + f_{\text{error}} T_S)},
\]

\[
SNR_m \approx \frac{\left(1 - \frac{\tau_{\text{error}}}{T_S}\right)^2}{\frac{N_0}{E_s (m)} + \frac{\tau_{\text{error}}^2}{T_S^2} + \frac{2\tau_{\text{error}}^2}{T_S^2} \sum_{n=0, n \neq m}^{N-1} \sin^2 \left(\frac{(n-m)\tau_{\text{error}}}{T_S}\right)}.
\]

Equation (2) presents the ICI caused by the frequency offset in the \( m \)-th carrier and Equation (3) presents ICI and ISI caused by the timing offset in the \( m \)-th carrier, when ISI is present in theFFT window. In these equations, \( f_{S} \) represents the OFDM symbol period, \( N \) represents the total number of carriers, \( E_s (m) \) is the \( m \)-th carrier average energy and \( N_0 \) represents the AWGN channel noise spectral density. It can be seen in Equations (2) and (3) that degradations caused by \( f_{\text{error}} \) and \( \tau_{\text{error}} \) are predominant. It is important to notice that when \( |\tau_{\text{error}}| \leq T_{CP} \) the timing error results only in a phase displacement, which can be easily compensated for by the channel estimator.

III. SYNCHRONIZATION PARAMETERS FOR IMPLEMENTATION

In order to implement timing and CFO synchronization in our system, we have chosen a maximum likelihood technique proposed in [13]. This technique allows us to jointly estimate the timing and CFO by means of the cyclic prefix correlation properties, as shown in Figure 3.

A classical synchronization approach uses the maximum likelihood (ML) criterion to estimate the \( f_{\text{error}} \) and \( \tau_{\text{error}} \), as presented in [10] and [13]. In [13], the estimated frequency offset \( \hat{f}_{\text{error}} \) and the estimated \( \hat{\tau}_{\text{error}} \), are obtained by the following equations
The correlation magnitude between the time-domain samples is a constant which depends on the SNR and represents the argument of a complex number, $\phi(n)$.

Obtained by the technique presented in [13], we can already filter the estimated timing and CFO values, as presented in Figure 4 and Figure 5. This approach would increase the system complexity, since it would include new synchronization algorithms and new control circuitry, for instance, an out-of-synch detection system to restart the acquisition mode. On the other hand, with some filtering applied to the estimated timing and CFO values, obtained by the technique presented in [13], we can already correct removal of the CP.

A. Implementation Details

Due to some system operations characteristics, we can further reduce the complexity of the technique presented in [13]. First of all, notice that there is a correlation coefficient $\rho$ that is a function of the SNR. Hence, for its calculation it is necessary to estimate the SNR and make one division, which is not a simple computational task. However, the value of $\rho$ is almost equal to one for small values of SNR (e.g., $12\mathrm{dB}$, $\rho = 0.94$). Thus, its impact on the performance is negligible.

The second simplification was done in the calculation of $\hat{\tau}_{\text{error}}$. Since the correlation value given by $\gamma(n)$ is a complex number, then the use of a modulus function as defined in (7) would require a square-root function. To further reduce the complexity, we have approximated this operation by the modulus of the real part plus the modulus of the imaginary part, as shown in Figure 6. For such approach the relative error is no greater than $\sqrt{2}$. Moreover, we have implemented the CFO compensation in closed-loop. Therefore, when the CFO is acquired, this imaginary part tends to zero and the resulting error also tends to zero. The search-step is used to find $\hat{\tau}_{\text{error}}$.

The correlation value given by $\gamma(n)$ is equal to one sample of the OFDM symbol, which is equal to $T = 63/512\mu s$. Any value for the timing offset smaller than the sample period can be compensated by the channel equalizer. The CFO correction procedure is shown in Figure 6.

Aiming at a simple but yet robust detection of the maximum value in Equation (7), we perform the block sum of $|\gamma(\hat{\tau}_{\text{error}})|^2 - \rho \phi(\hat{\tau}_{\text{error}})$ over four successive OFDM symbols, as presented in Figure 4. The simulated results for this technique are shown in Figure 8. Such a technique assumes that the timing offset variation during this period is smaller than $T_S$. The value $\hat{\tau}_{\text{error}}$ controls the timing by choosing the appropriate position of the FFT window and the correct removal of the CP.

We also provide a mechanism to synchronize the timing update with the Alamouti codeword. This had to be done because the channel estimation is performed at codeword rate, implying that any update of the timing instant inside the codeword would break its orthogonality.

The estimated CFO error $\hat{f}_{\text{error}}$ is fed into a filter. This filter is composed of a scaled digital integrator and a scaled DDS.
直接路径。滤波器输出然后被馈送到 DDS（直接数字合成器），它扮演一个模拟 VCO（电压控制振荡器）的角色。DDS 生成用于应用到接收的共轭相位和正交信号成分的余弦和正弦信号，纠正 CFO。所组成的 CFO 估计、滤波器、DDS 和 CFO 纠正的循环被称为数字相位锁定环（DPLL）。

在下面，我们展示了在巴西数字电视测试[1]（表 I）中使用的某些信道的性能曲线。
TABLE II
RESOURCE UTILIZATION SUMMARY FOR THE PRESENTED RECEIVER PROTOTYPE.

<table>
<thead>
<tr>
<th>Resource</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Occupied Slices</td>
<td>13063</td>
<td>15360</td>
<td>85%</td>
</tr>
<tr>
<td>Number of BRAM (FIFO16)</td>
<td>94</td>
<td>192</td>
<td>48%</td>
</tr>
<tr>
<td>Number of DSP48s</td>
<td>47</td>
<td>192</td>
<td>24%</td>
</tr>
</tbody>
</table>

The device utilization summary is presented in Table II for the demodulator design. Most of the FPGA’s BRAMs (58 of 94 BRAMs) are used for the synchronization algorithms, while most of the logic elements (11132 of 13063 slices) are used for demodulation, space-time decoding and channel estimation tasks.

The synchronization algorithm is responsible for the large BRAM usage because of the correlation between N samples apart and the block sum average over four OFDM symbols. This hardware implementation strategy was of especial interest to us due to the large number of embedded BRAMs in the chosen FPGA. If these BRAMs were not available, a large number of slices (a measure of logical devices for Xilinx’s FPGAs) would be consumed to execute memory functionalities. Such an approach would be hardly feasible due to the already large usage of the slices (around 73%) by the other receiver functionalities.

The first proof of concept for the MI-SBTVD was performed in January 2006. The RF stage was assembled for the transmitter front-end using mixers, power amplifiers and oscillators to transmit a DTV signal on a 512.8137 MHz carrier. The RF stage for the receiver front-end was assembled using a down-converter test equipment designed by Linear Equipments. The IF stage received an analog signal centered at 8.126984 MHz and sampled it at a rate of four times this frequency. The external clock reference for the prototype was set to a frequency of 65.015873 MHz. For this first proof of concept the implemented synchronism scheme worked nicely.

VI. CONCLUSIONS

This paper presented the synchronism scheme designed, simulated and implemented for the MI-SBTVD. We have shown the design aspects, simulation results and details of the hardware implementation over FPGA. Additional performance improvements are being investigated by fine-tuning the estimated parameters and by studying a superior bit allocation for the quantized variables. Furthermore, a more robust technique is also under investigation for application in mobile receivers.

REFERENCES